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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/811,892

03/30/2004

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1793.1184

1320

21171 7590 06/21/2007  
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EXAMINER

SITTA, GRANT

ART UNIT

PAPER NUMBER

2629

MAIL DATE

DELIVERY MODE

06/21/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

**Application No.**

10/811,892

**Applicant(s)**

KIM, EUN-SUP

**Examiner**

Grant D. Sitta

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 March 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 8/05/2004 3/30/2004.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the “checking last until the second horizontal synchronization signal is generated” Claim 11, lines 1-2 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings also fail to clearly show claims 12 and 26

***Specification***

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 11.

***Claim Rejections - 35 USC § 112***

1. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Examiner notes the “determining” and the “checking operations” determine if the user has changed the display mode. How can these steps be skipped because the user may change the mode in the next instance?

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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3. Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Park et al (7,098,903) hereinafter, Park.

4. In regards to claim 13, driving the backlights in synchronization with a first synchronization signal (fig. 3 (110) driven according to various inputs) in a video determining whether a display mode (Fig. 3, DVI, S-Video, Analog) has been changed (Examiner notes since the input has various inputs it is inherent it has a way to determine which mode to display); stopping the driving (Fig. 3 "Backlight ON/OFF"), if the display mode is changed; checking whether the display mode change is completed; and resuming driving the backlights in synchronization with a second synchronization signal (The synchronization signal of the mode changed to for example DVI to S-Video) in a video signal if the display mode change is completed (col. 5 lines 25-65).

5. Claims 19 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoo et al (2003/0214478) hereinafter Yoo.

6. In regards to claim 19, A panel ([0011], panel) and an inverter ([0009], inverter) in a liquid crystal display having backlights, which are synchronized with one another to avoid oscillatory interference there between and to remove noise from a screen,

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wherein the inverter is turned off during a display mode change to prevent the backlights from being turned off (Fig. 12 [148]-[152]).

7. In regards to claim 20, see claim 19

8. Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Herrmann.

9. In regards to claim 21, extracting a first synchronization signal (col. 20, lines 50-55) from the sampled digital video signals (col. 2 lines 38-70); driving the backlights in synchronization with the first synchronization signal (col. 20, lines 50-55); stopping the driving if a display mode of the liquid crystal display is changed (col. 3, lines 50-55); extracting a second synchronization signal from the sampled digital video signals; driving the backlights in synchronization with the second synchronization signal if the changing of the display mode is determined to be completed (col. 3, lines 50-65).

***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claim 1,2,3, 6,7,8 and 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al (7,098,903) hereinafter, Park.

1. A liquid crystal display (fig. 1), having a liquid crystal panel (fig. 1 ((230) "flat panel display panel")) and backlights (col. 5, lines 65-70)), comprising:

a signal converter (Fig. 1 (310)) to convert selectively input analogue video signals into digital video (Fig. 1 (ADC)) signals in synchronization with a first predetermined sampling clock signal (col. 5, lines 30-36));

a scaler (fig. 1 (340) lines 27-32) to sample the digital video signals at a preset resolution in synchronization with a second predetermined sampling clock signal, and to extract a horizontal synchronization signal from the sampled digital video signals (col. 5, lines 30-36)); Examiner notes a horizontal synchronization signal is carried on the input signal and must be extracted to display formats, such as VGA., and is an inherent element in displays.

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a panel driver (fig. 1 (220)) to display the digital video signals on the liquid crystal panel (fig. 1 ((230) "flat panel display panel"));

a controller (fig. 1 (340) lines 27-32) to detect the extracted horizontal synchronization signal from the digital video signals to determine a display mode (col. 5, lines 30-36)), to output the first and second predetermined sampling clock signals to the signal converter and the scaler (fig. 1 (340) lines 27-32), respectively, according to the determined display mode, and to generate inverter on/off signals (Fig. 3 signal to (110)) whenever the display mode is changed (col. 2, lines 5-10) and (col. 5 25-45). Examiner notes while the reference does not explicitly say the horizontal synchronization signal is used to drive the scaler and signal converter, one skilled in the art will recognize a clock is needed for both these devices and the will be set to the horizontal synchronization signal.

an inverter (fig. 3 (110)) to drive the backlights (col. 5, lines 65-70)), in synchronization with the detected horizontal synchronization signal (col. 5, lines 40-45) and the inverter on/off signals (fig. 3 "backlight on/off").

2. In regards to claim 2, a pulse width modulator to generate pulse width modulation signals (fig. 3 (110)), which are synchronized with the horizontal synchronization signal (fig. 3 (340)), and to turn the pulse width modulation signals on or off (fig. 3 "backlight on/off") according to the inverter on/off signals generated by the controller (fig. 3 (340)); a switching transformer to switch a power supply on or off according to the pulse width modulation signals; and a lamp which radiates light using the power supplied by the



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switching transformer (fig. 3 (110)). Examiner notes that it is inherent that an inverter will have a switching transformer. Examiner also notes that pulse width modulation is an obvious matter of design choice to use pulse width modulation with an inverter, since applicant has not disclosed that having the pulse width modulation solves any stated problem or is for any particular purpose and it appears that the inverter would perform equally well with other forms of modulation. (See "Pulse Width Modulation (PWM) Basics" Under "3. Regular Sampled PWM" where "an inverter can generate a PWM signal")

3. In regards to claim 3, the controller generates and outputs the inverter off signals to the inverter when the display mode is changed, and continues generating and outputting the inverter off signals until the horizontal synchronization signal is detected (col. 3, lines 24-30).

4. In regards to claim 6, controlling (fig. 3 (340)) an inverter (fig. 3 (110)) to drive the backlights in synchronization with a first horizontal synchronization signal (clock inherent) in a digital video signal (Fig. 1 input from (320) "Digital interface") when video signals are input; determining whether a display mode has been changed (col. 2 lines 5-10 "various input signals"); inputting an inverter (fig. 3 (110)) off signal to the inverter (Fig. 3 "Backlight ON/OFF"), if the display mode is changed (col. 2 lines 5-10 "various input signals"), to control the inverter (fig. 3 (110)) to not drive the backlights; checking whether the display mode change is completed; and inputting an inverter on signal to

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the inverter if the display mode change is completed so as to control the inverter to drive the backlights in synchronization with a second horizontal synchronization signal (col. 3, lines 20-30 "signals").

5. In regards to claim 7, checking if the display mode change is not completed. (col. 3, lines 22-30) Examiner it would have been obvious to one skilled in the art to have the input device continually check to see if the input change is complete.

6. In regards to claim 8, further comprising skipping the determining the inputting the inverter off signal, and the checking operations if the user has not changed the display mode.

7. In regards to claim 10, wherein the determining comprises determining whether the display mode is changed from a PC (analog) to that of a DTV (DVI-D).

8. Claims 4 and 5 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ogoro (US 6,891,525) hereinafter, Ogoro.

9. In regards to claim 4, where a display mode (abstract "operation mode") changes while video signals are displayed (Abstract "data input mode"); and applying backlight

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off signals (Abstract "backlight is reduced" Examiner notes it could easily be reduced to zero) to the inverter (fig. 1 (103) inherent with D.C. powered backlights) while the display mode is changing (Fig. 7 S56), and applying backlight on signals to the inverter when a horizontal synchronization signal is detected (col. 2 60-70) and (col. 8 lines 35-45).

10. In regards to claim 5, wherein the horizontal synchronization signal begins to cause a transient effect when the display mode is changed (col. 4, lines 15-25).

Examiner notes it is inherent to have a transient effect when a mode is changed until the clock is reset.

11. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Ogoro.

12.

13. In regards to claim 11, Park discloses the limitations of claim 6

Park differs from the claimed invention in that Park does not disclose wherein the checking last until the second horizontal synchronization signal is generated

However, Ogoro teaches a system and method for wherein the checking last until the second horizontal synchronization signal is generated "(Fig. 7 col. 7-8, lines 60-35 of Ogoro).).

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It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Park to include the use of checking until the second signal is generated as taught by Ogoro in order for "detecting a currently set operation mode..." as stated in (Fig. 7 col. 2, lines 20-30 of Ogoro).

14. In regards to claim 12, where the checking comprises determining whether the second horizontal synchronization signal exist in the video signals. (Fig. 7 col. 7-8, lines 60-35 of Ogoro).

15. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park, in view of Anderson et. al (US 6,678,005) hereinafter, Anderson.

16. In regards to claim 9, Park discloses the limitations of claim 1

Park differs from the claimed invention in that Park does not disclose

However, Anderson teaches a system and method for recognizing key signals (Examiner notes key signals will be necessary when the user is prompted with the choice) as display mode change signals if the video signals are those of a PC (Abstract "PC") and are displayed (fig. 3, (370)) when the user inputs the key signals to change the video signals (fig. 3 (360)). (col. 2, lines 20-50 of Anderson).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Park to include the use of means recognizing key signals as display mode change when the video signal are those of a PC as taught by Anderson in order

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to "...accommodate for concurrent presence of multiple video signals in a PC or TV environment." as stated in (col. 2, lines 15-20 of Anderson).

17. Claim 14 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Park.

18. In regards to claim 14, repeating the checking if the display mode change is not complete (fig. 3). Park discloses a display device with multiple inputs having all the features claimed except for the specific checking if the display mode is not changed. Although it the "checking" is not explicitly stated it would have been obvious to one skilled in the art since a clock is an inherent part of a display device and would be necessary to determine when an input device is connected to the display device.

19. Claims 15, 16, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park, in view of Ogoro.

20. In regards to claim 15, Park discloses the limitations of Ogoro

Park differs from the claimed invention in that Park does not explicitly disclose skipping the determining, the inputting, the stopping, and the checking operations if the display mode is not changed.

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However, Ogoro teaches a system and method for "mode setting selecting"(Fig. 7 col. 7-8, lines 60-35 of Ogoro).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Park to include the use of "mode setting selecting" as taught by Ogoro in order to provide for mode selection and lowering power consumption as stated in (col. 2, lines 15-65 of Ogoro).

21. In regards to claim 16, determining comprises recognizing key signals as display mode change signals. (col. 3-4, lines 70-5 Ogoro).

22. In regards to claim 17, the checking last until the second synchronization signal is generated (Fig. 7 col. 7-8, lines 60-35).

23. In regards to claim 18, where the checking comprises determining whether the synchronization signal exist in the video signal (col. 4, lines 20-65).

24. Claims 22,23,24,25 and 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loveridge et al (US 6,545,688) hereinafter Loveridge, in view of Cui et. al (US PUB 7,119,786) hereinafter, Cui.

25. In regards to claim 22, Loveridge discloses the limitations of a signal converter to convert a video signal into a digital video signal in synchronization with a first sampling

clock signal (fig. 3, col. 8, lines 30-40);

a scaler to sample the digital video signal in synchronization with a second sampling clock signal (fig. 3 (370)), and to extract a first synchronization signal therefrom (fig. 3, col. 8, lines 19-30, "HSYNC");

a panel driver to display (fig. 1b (160)) the digital video signals on the liquid crystal panel (fig. 1b (170)); a controller to detect the synchronization signal (col. 8, lines 19-30, "HSYNC") from the digital video signal to determine a display mode (Examiner notes "display mode" is very broad and can encompass such thing as a change in scale.), to output the first and second sampling clock signals ("The specific sampling time points may be controlled by a source clock..." since there are multiple points there must be more than one clock) to the signal converter and the scaler (col. 8, lines 5-50), respectively, according to the determined display mode, and to generate inverter on/off signals whenever the display mode is changed;

Loveridge differs from the claimed invention in that Loveridge does not disclose an inverter to drive the backlights in synchronization with a second synchronization signal and the inverter on/off signals.

However, Cui teaches a system and method for an inverter to drive a backlight in synchronization with a second synchronization signal and the inverter on/off signal (Fig. 5 col. 5, lines lines 35-70 of Cui).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Loveridge to include the use of an inverter with the backlight in synchronization with a second signal and on/off signal as taught by Cui in order to

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maintain a display image quality regardless of variances in backlight brightness of a flat-panel display..." as stated in (col. 2, lines 55-60 of Cui).

26. In regards to claim 23, wherein the controller determines a display mode (fig. 3 (360), col. 9, lines 30-37, Loveridge).

27. In regards to claim 24, the controller outputs the first and second sampling clock signals to the signal convert (Fig. 3 (380) and (390)) and the scaler (Fig. 3 370) respectfully according to the determined display mode (Fig. 3 col. 9, lines 28-36, Loveridge).

28. In regards to claim 25, wherein the inverter comprises a pulse width modulator to generate pulse width modulations signals synchronized with the first synchronization signal to turn the pulse width modulation signals on and off according to the inverter on/off signals generated by the modulator. (Fig. 5, col. 35-70, Cui "Power Sequencer" is a PWM (See Patent 6,766,222 Fig. 2)).

29. In regards to claim 26, wherein the inverter further comprises a switching transformer to switch a power supply on or off according to the pulse width modulation signals input from the pulse width modulator. (Fig. 5, col. 35-70, Cui "Power Sequencer" is a PWM Inherent in a "Power Sequencer" (See Patent 6,766,222 Fig. 3)).



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30. In regards to claim 27, wherein the inverter further comprises a lamp to radiate light using the power supplied by the switching transformer. (Fig. 5, col. 35-70, Cui).

Examiner notes the Applicant is merely claiming an inverter built into the backlight and would have been obvious to one skilled in the art.

31. In regards to claim 28, the controller generates and outputs inverter off signals to the inverter when the display mode is changed, and continues generating and outputting inverter off signals until the second synchronization signal is detected. (Fig. 5 "D" remote on signal and remote off signal).

32. In regards to claim 29, see claim 22 and an inverter which is synchronized with the liquid crystal panel to avoid oscillatory interference therebetween, to drive the backlight in synchronization signal with a second synchronization signal and the inverter on/off signals (fig. 5 col. 5, lines 35-70, "D" remote on and off).

### **Inquiry**


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant D. Sitta whose telephone number is 571-270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-270-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Grant D. Sitta  
May 15, 2007

  
AMARE MENGISTU  
SUPERVISORY PATENT EXAMINER